PTO-1449 REPRODUCED

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION

February 15, 2007

(Use several sheets if necessary)

ATTORNEY DOCKET NO.	APPLICATION NO.	
2037.1002-003	10/032,431	
FIRST NAMED INVENTOR	FILING DATE	
Richard C. Foss	December 21, 2001	
EXAMINER	CONFIRMATION NO.	GROUP
Dinh, Tan X.	8755	2627

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF. NO.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
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	A57	5,444,203	08-22-1995	Gunnarsson
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	C4	Adler, E., "The Evolution of IBM CMOS DRAM Technology," *IBM J. Res. Develop.*, Vol. 39 No. 1/2, January/March 1995, p. 169.
	C5	Anceau, "A Synchronous Approach for Clocking VLSI Systems," *IEEE Journal of Solid-State Circuits*, Vol. SC-17, No. 1 (Feb. 1982).
	C6	Chen, "Designing On-Chip Clock Generators," Circuits and Devices, July, 1992, pp. 32-36.
	C7	Chou, Shizuo, *et al.*, "A 60-ns 16M-bit DRAM With a Minimized Sensing Delay Caused by Bit-Line Stray Capacitance," *IEEE Journal of Solid State Circuits*, Vol. 24, No. 5, Oct. 1989, pp. 1176-1178.
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	C10	Gasbarro, *et al.*, "Techniques for Characterizing DRAMS With a 500 MHz Interface," International Test Conference, Oct. 1994, pp. 516-525.
	C11	Gasbarro, "Testing High Speed DRAMS," International Test Conference, Oct. 1994, p. 361.
	C12	Gillingham, Peter, *et al.*, "High-Speed, High-Reliability Circuit Design for Megabit DRAM," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 8, August 1991, pp. 1171-1175
	C13	Horowitz, Mark, "Clocking Strategies in High Performance Processors," *1992 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 50-53.
	C14	Horowitz, M., *et al.*, "PLL Design for a 500 MB/s Interface," ISSCC Digest of Technical Papers (Feb. 1993)
	C15	Johnson, *et al.*, "A Variable Delay Line PLL for CPU-Coprocessor Synchronization," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, October, 1988, pp. 1218-1223.
	C16	Kim, S., *et al.*, "A Pseudo-Synchronous Skew-Insensitive I/O Scheme for High Bandwidth Memories," *1994 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 41-42.
↓	C17	Menasce, V., *et al.*, "A Fully Digital Phase Locked Loop," Canadian Conference on VLSI, Oct. 1990, pp. 9.4.1 – 9.4.8.
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	C20	Przybylski, Steven, New DRAM Technologies, A Comprehensive Analysis of the New Architectures, MicroDesign Resources, Sebastopol, CA, (1994).
	C21	Rambus document RM 2744932-33, details Rambus making certain technical information publicly available on the internet in November 1993.
	C22	Rambus Product Catalog, by Rambus, Inc., 1993.
	C23	RDRAM Reference Manual, by Rambus, Inc., 1993.
	C24	Schanke, Morten, "Proposal for Clock Distribution in SCI," May 5, 1989.
	C25	Sidiropoulos, Stefanos, *et al.*, "A CMOS 500 Mbps/pin synchronous point to point link interface," *1994 Symposium on VLSI Circuits, Digest of Technical Papers*, pp. 43-44.
	C26	Wagner, Kenneth, *et al.*, "Testable Programmable Digital Clock Pulse Control Elements," *International Test Conference 1993*, pp. 902 – 909.
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	C28	Deposition of Thomas Vogelsang, dated 6/4/04.
	C29	MOSAID's Complaint for Patent Infringement and Jury Demand, filed 4/6/05, *Mosaid Technologies, Inc. v. Infineon North America Corp., et al*, Civil Action No. 05-00120 (E. D. TX).
	C30	Defendants' [Infineons'] Answer and Counterclaims, filed 6/15/05, *Mosaid Technologies, Inc. v. Infineon North America Corp., et al*, Civil Action No. 05-00120 (E. D. TX).
	C31	MOSAID's Reply to Infineon's Counterclaims, filed 6/29/05, *Mosaid Technologies, Inc. v. Infineon North America Corp., et al*, Civil Action No. 05-00120 (E. D. TX).
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/TD/	C34	[MOSAID's] First Amended Complaint for Patent Infringement and Jury Demand, filed 3/30/06, *Mosaid Technologies, Inc. v. Infineon North America Corp., et al*, Civil Action No. 05-00120 (E. D. TX).
	C35	[MOSAID's] Second Amended Complaint for Patent Infringement, filed 4/20/06, *Mosaid Technologies, Inc. v. Infineon North America Corp., et al*, Civil Action No. 05-00120 (E. D. TX).
	C36	[Infineons'] Answer and Counterclaims to Second Amended Complaint, filed 5/4/06, *Mosaid Technologies, Inc. v. Infineon North America Corp., et al*, Civil Action No. 05-00120 (E. D. TX).
	C37	Micron's Complaint for Declaratory Judgment, filed 7/24/06, *Micron Technology, Inc. v. Mosaid Technologies, Incorporated*, Civil Action No. 06-04496 (N.D.CA).
/TD/	C38	Order Granting Mosaid's Motion to Dismiss for Lack of Subject Matter Jurisdiction, entered 10/23/06, *Micron Technology, Inc. v. Mosaid Technologies, Incorporated*, Civil Action No. 06-04496 (N.D.CA).

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